

Claims

1. A router for routing signals between a host (3) and a plurality of processors (X10) in a system (1), characterised in that, the router
5 comprises:

a host channel (5) for linking the router to the host;

a plurality of processor channels (6) each for linking the router to
10 one of the processors (X10);

routing means (15) comprising means for routing host commands to a selected processor and for routing responses from the selected processor to the host (3); and
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selection means (19) in the router (2) for selecting a processor (X10) by monitoring the host commands, identifying a host selection command by detecting a flag in the command, and reading an address for a selected processor in the host selection
20 command.

2. A router as claimed in claim 1, wherein the selection means (19) comprises means for reading an address from an address field in a host selection command.
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3. A router as claimed in claim 1, wherein the router comprises means for synchronising with a selected processor (X10) by monitoring an incoming command stream and an outgoing response, and for

determining the total width of the fields of a host command, specific to width configurations of the processor.

4. A router as claimed in claim 3, wherein the synchronisation means (19)
5 comprises means for determining the combined data path width and memory width of the selected processor according to data path and memory field widths in a host command.
- 10 5. A router as claimed in claim 3, wherein the synchronisation means (19) comprises means for monitoring a next host command following a selection host command to determine a width parameter of the selected processor.
- 15 6. A router as claimed in claim 1, wherein the routing means comprises a multiplexer (15) comprising means for routing communication between the host and the selected processor (X10), and the selection means comprises monitoring logic (19) for monitoring incoming host commands and writing a selected processor address to a register (20) for said multiplexer.
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7. A router as claimed in claim 6, wherein the synchronisation means comprises monitoring logic (19) for monitoring incoming host commands and outgoing responses, and for writing synchronisation data to a register (20) for said multiplexer (15).
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8. A router as claimed in claim 6, wherein said multiplexer (15) is connected to processor channels (6) for data processors, and the router comprises a switch (16) comprising means for acting in response to a

control input from the host (3) to route host commands to control processors (18), bypassing the multiplexer (15).

5 9. A router as claimed in claim 1, wherein the router (2) and the processors (X10) reside on a single system-on-chip integrated circuit.

10 10. A router as claimed in claim 1, wherein the host commands are debug host commands, and the router comprises means for routing debug responses to the host.

10 11. A system-on-chip integrated circuit (1) comprising:

a plurality of data processors (X10);

15 at least one control processor (18);

a router (2) for routing signals between on external host (3) and said processors (X10), the router comprising:-

20 a host channel (5) for linking the router to the host (3);

a plurality of processor channels (6) each for linking the router (2) to one of the data processors (X10);

25 routing means (15) comprises means for routing signals between a selected data processor (X10) and the host;

selection means comprising means for monitoring incoming host commands on the host channel (5) to identify a host selection

command, for reading an address of a selected data processor from an identified host selection command, and for informing (19, 20) the routing means (15) of the selected data processor address;

5 synchronisation means (19) comprising means for monitoring incoming host commands on the host channel (5) and outgoing responses from the data processor, for determining width of a field of a host command, and for determining a combined width parameter of the selected data processor according to said field width, and for informing the routing means (15) of the width parameter;

10 means in the routing means (15) for synchronising signals between the host and the selected data processor according to said width parameter; and

15 a switch (16) comprising means for bypassing host command signals received on the host channel (5) from the routing means (15), and for routing them directly to the control processor (18).

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12. A system-on-chip integrated circuit as claimed in claim 11, wherein said switch (16) comprises means for bypassing said signals in response to a control input from the host.